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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/648,919 | 08/27/2003 | Shenggao Li | P16582 | 5068 |

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| EXAMINER | |
|---|---|
| SHINGLETON, MICHAEL B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2817 | |

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/648,919 | LI | |
| | Examiner | Art Unit | |
| | Michael B. Shingleton | 2817 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,2,11-13 and 17-22* is/are rejected.

7)☒ Claim(s) *3-10 and 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 11 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yabe 2001/0043123 (Yabe).

Figure 6-8 and the relevant text of Yabe discloses a ring oscillator for use in a pll circuit having a plurality of delay cells 10a coupled in series as a ring (Ring oscillator) and a replica cell 11 that includes a differential pair of transistors. Note the diode connected NMOS transistor in 2a and the diode connected NMOS transistor in 1a. Also note that these transistors have their sources i.e. "third terminals" connected to each other. The replica cell outputs a bias signal at the output of element 12. Note that this bias signal biases transistors that include Q10 and Q6. The diode connection is what applicant describes as the second terminal connected to the first. Q9 and Q8 met the first and second active resistors for as described by applicant FETs forms active resistors.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yabe 2001/0043123 (Yabe) in view of Iravani 5,936,476 (Iravani).

Figure 6-8 and the relevant text of Yabe discloses a ring oscillator for use in a pll circuit having a plurality of delay cells 10a coupled in series as a ring (Ring oscillator) and a replica cell 11 that includes a differential pair of transistors. Note the diode connected NMOS transistor in 2a and the diode connected NMOS transistor in 1a. The replica cell outputs a bias signal at the output of element 12. Note that this bias signal biases transistors that include Q10 and Q6. The diode connection is what applicant describes as the second terminal connected to the first. Q9 and Q8 met the first and second active resistors for as described by applicant FETs forms active resistors. The operational amplifier of Yabe fails to have the inverting input coupled to the replica cell whereas the non-inverting terminal is coupled to Vref. Note that the VCO of Yabe provides an input to the pll (phase locked loop) in the conventional manner. Yabe also fails to disclose the use of the circuit in an optical transmitter. Clearly Yabe is a component of a larger system.

One well known alternative and art recognized equivalent biasing arrangement to control the biasing of the delay cells and thus the frequency is by an operational amplifier wherein the inverting terminal is connected to the replica circuit and the output is connected to active resistors that control the current through the delay cells as taught by Iravani (See Figure 2).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replace the operational amplifier circuit of Yabe with one that has an operational amplifier wherein the inverting terminal is connected to the drain terminal of the replica circuit and the output is connected to active resistors that control the current through the delay cells given the art recognized equivalence as taught by Iravani.

Yabe is a component of a larger system. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the clock of that made obvious above in a conventional optical transmitter arrangement that includes first and second pll's because, as the references are silent on the exact use of the component one of ordinary skill in the art would have been

motivated to use the component in any art-recognized system that employs pll's or clocks such as the conventional optical transmitter arrangement that includes first and second pll's. Note that applicant describes the invention as being in the replica cell and not the optical transmitter arrangement. Accordingly, the basic optical transmitter arrangement claimed is seen as conventional.

Claims 12, 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yabe 2001/0043123 (Yabe).

Figure 6-8 and the relevant text of Yabe discloses a ring oscillator for use in a pll circuit having a plurality of delay cells 10a coupled in series as a ring (Ring oscillator) and a replica cell 11 that includes a differential pair of transistors. Note the diode connected NMOS transistor in 2a and the diode connected NMOS transistor in 1a. The replica cell outputs a bias signal at the output of element 12. Note that this bias signal biases transistors that include Q10 and Q6. The diode connection is what applicant describes as the second terminal connected to the first. Q9 and Q8 met the first and second active resistors for as described by applicant FETs forms active resistors. The operational amplifier of Yabe fails to have the inverting input coupled to the replica cell whereas the non-inverting terminal is coupled to Vref. Note that the VCO of Yabe provides an input to the pll (phase locked loop) in the conventional manner. Yabe also fails to disclose the use of the circuit in an optical transmitter. Clearly Yabe is a clearly a component of a larger system.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the clock of that made obvious above in a conventional optical transmitter arrangement that includes first and second pll's because, as the references are silent on the exact use of the component one of ordinary skill in the art would have been motivated to use the component in any art-recognized system that employs pll's or clocks such as the conventional optical transmitter arrangement that includes first and second pll's. Note that applicant describes the invention

as being in the replica cell and not the optical transmitter arrangement. Accordingly, the basic optical transmitter arrangement claimed is seen as conventional.

Claims 3-10 and 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's arguments filed 1-27-2005 have been fully considered but they are not persuasive. Applicant has amended the claims to recite the first transistor also having a third terminal and the second transistor also having a third terminal coupled to the third terminal of the first transistor. Applicant alleges that the third terminals of the first and second transistors of the Yabe reference US 2001/0043123 are not coupled together and that the first and second transistors of the Yabe reference do not "constitute a "differential pair", since their source terminals are not coupled together". The examiner respectfully disagrees. The diode connected NMOS transistors of elements 1a and 2a of Yabe do have their "third" terminals connected together. In particular note that the third terminals of these transistors are connected together via the two transistors that have their gates directed connected to the line "CONT". Because of this, it is proper to refer to these first and second transistors as a "differential pair". Note that the current from these transistors are combined and then passed to the ground terminal. Furthermore, it appears that applicant may be utilizing the term "coupled" in too narrow a sense. Coupled does not mean the same as directly connected. There can be elements between the two items coupled together. An electrical generator plant is coupled to the common light bulb in a home even though there are transformers and switches in between. Applicant also makes a statement that "it seems to applicant that the variable impedance loads 1a and 2a correspond in function to the active resistors 152 and 156 in FIG. 1". This statement of belief does not address how the claimed structure differs if at all from the prior art. As noted

above the first and second transistors of Yabe can be considered a differential pair. Note that the transistors Q9 and Q8 of Yabe are connected between a power supply and the respective drain terminals of the first and second transistors. Thus these transistors form the "active resistor elements" in Yabe as claimed in the instant application. It does not appear that the functions that applicant is apparently implying in his remarks are part of the claimed invention. The examiner must give the broadest reasonable interpretation to the claims and since the instant application lacks any specific definition of terms, the plain meaning of the terms that appear in the claims have been given (See MPEP 2111 and 2111.01). Applicant also remarks that the signal $VCO_{in}$ is the control voltage for the VCO and controls the frequency of oscillation as per column 4, around line 42 of Irvani and then states "Thus, the amplifier 201 does not receive a reference signal and does not set the common mode output voltage for the oscillator". Just because the signal $VCO_{in}$ controls the frequency of the VCO does not mean that it cannot also be a reference voltage to set the common mode output voltage of the oscillator. Note that the active resistor elements of Iravani are of the same type as that of applicant's invention. The examiner does not see a limitation in the claims that would exclude the VCO voltage that controls the frequency from forming the reference signal as recited by the claims. Applicant points out that the output of amplifier 12 of Yabe is not directly connected to the active resistors 1a and 2a. The examiner has identified in the previous rejection that the output of element 12 of Yabe is applied to transistors Q10 and Q6. Thus the examiner agrees with applicant that the Yabe reference does not anticpate the claimed invention of claim 17 of the instant application. However, the rejection was one of obviousness wherein it is what the combined teachings of references suggest. The rejection was one that replaced the biasing of Yabe with that of the biasing of Iravani. Applicant in his remarks above points out that only one signal can be used i.e. $VCO_{in}$ that controls the active resistor elements connected to Vdd. This actually provides for further motivation for one to make the substitution and that is only one signal is needed for the VCO and the reference signal as taught by Iravani. The examiner still contends that the replacement of one baising

arrangement for that of another would have been obvious to one of ordinary skill in the art because of the art recognized equivalence of these arrangements.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
April 15, 2005

Michael B Shingleton
Primary Examiner
Group Art Unit 2817